location, where d is less than d_{max}, said first and second locations being separated by a predetermined horizontal distance;

a source region of said first conductivity type formed in said epitaxial layer above a portion of said body region, said portion of said body region being located between said second location and said source region; and

a trench formed in said epitaxial layer, having substantially vertical side walls, and extending from said top surface of said epitaxial layer to a depth d_{tr} less than said depth d_{max} and greater than said depth d, said trench being (i) closer to said second location than to said first location and (ii) horizontally adjacent to said source region; wherein breakdown in said trench DMOS transistor cell occurs across said epitaxial layer at a position closer to said first location than to said second location.

#1 Concl'd

2 1
~~18.~~ (Amended) A trench DMOS transistor cell as in Claim ~~17~~ wherein said body region has a portion exposed at said top surface of said epitaxial layer.

3 2
~~19.~~ (Amended) A trench DMOS transistor cell as in Claim ~~18~~ wherein said source region has a portion exposed at said top surface of said epitaxial layer.

4 1
~~20.~~ (Twice amended) A trench DMOS transistor cell as in Claim ~~17~~ wherein depth d_{tr} is less than d_{max} by an amount sufficient to cause semiconductor surface breakdown to occur at a location closer to said first location than to said second location.

6 1
~~21.~~ (Twice amended) A trench DMOS transistor cell as in Claim ~~17~~ wherein said epitaxial layer has a thickness d_{epi} small enough to cause semiconductor surface breakdown to occur at a location closer to said first location than to said second location.

6 1
~~22.~~ (Amended) A trench DMOS transistor cell as in Claim ~~17~~ wherein said trench, when viewed from above said top surface of said epitaxial structure, is polygonal and has a number of sides greater than four.

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7 6
~~23.~~ (Amended) A trench DMOS transistor cell as in Claim ~~22~~ wherein said number of sides is six.

8
25. (Amended) A trench DMOS transistor cell as in Claim 17 wherein said trench contains polysilicon isolated from said source and body regions by a layer of gate oxide.

9
26. (Twice amended) A trench DMOS transistor cell as in Claim 21 wherein said gate oxide has a thickness sufficient to cause semiconductor breakdown to occur at a location closer to said first location than to said second location.

10
27. (Unchanged) A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an closed cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

#2

11
28. (Unchanged) A semiconductor wafer comprising a predetermined number of trench DMOS transistor cells in an open cell configuration, each trench DMOS transistor cell in said semiconductor wafer being a DMOS trench transistor cell as recited in Claim 17.

12
29. (Twice amended) A trench DMOS transistor cell as in Claim 17 wherein said substrate has a dopant concentration higher than said initial dopant concentration of said epitaxial layer, said substrate and said epitaxial layer forming respectively drain and drift regions of said trench DMOS transistor cell.

13
30. (Four times amended) A trench DMOS transistor cell comprising:

a substrate of semiconductor material of a first electrical conductivity type having a top surface;

a first covering layer of semiconductor material of said first electrical conductivity type, said first covering layer (i) having a dopant concentration less than that of said substrate, (ii) having a top surface and (iii) being contiguous to and overlying the top surface of the substrate;

a second covering layer of semiconductor material of a second electrical conductivity type opposite to said first electrical conductivity type having a top surface and being contiguous to the top surface of the first covering layer and extending vertically downward from the top surface of the first covering layer into an upper portion of the first covering layer;

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a third covering layer of semiconductor material of said first electrical conductivity type having a top surface and being contiguous to and partly overlying the top surface of the second covering layer where the maximum depth of the second covering layer relative to the top surface of the third covering layer is a depth d_1;

a trench, having side walls and a bottom wall, said side walls extending vertically downward from the top surface of the third covering layer through the third and second covering layers and through a portion of, but not all of, the first covering layer, where the trench has a maximum depth relative to the top surface of the third covering layer equal to a second depth d_2 less than d_1;

a layer of oxide positioned within the trench and contiguous to the bottom walls and side walls of the trench so that portions of the trench are filled with the oxide layer;

electrically conducting semiconductor material contiguous to the oxide layer and positioned within the trench so that the oxide layer lies between the electrically conducting semiconductor material and the bottom and side walls of the trench; and

three electrodes electrically coupled to the electrically conducting semiconductor material in the trench, to the third covering layer and to the substrate, respectively; wherein junction breakdown occurs away from the trench and into a portion of the second covering layer.

14 ~~31.~~ (Twice amended) A trench DMOS transistor cell as in Claim 13 ~~30~~ wherein said trench comprises rounded edges of oxidized material.

15 ~~32.~~ (Thrice amended) A trench DMOS transistor cell comprising:

a substrate;

an epitaxial layer above the substrate;

a trench in the epitaxial layer, the trench having substantially vertical side walls and having a predetermined depth d_{tr}; and

a body region in the epitaxial layer, the body region having a predetermined maximum depth d_{max}; wherein depth d_{tr} is less than depth d_{max}, and wherein junction breakdown occurs away from the trench and into the epitaxial layer.

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16 ~~33~~. (Amended) A trench DMOS transistor cell as in Claim 15 ~~32~~ wherein the substrate is of a first conductivity type, the epitaxial layer is of said first conductivity type and the body region is of a second conductivity type opposite to said first conductivity type.

17 ~~34~~. (Amended) A trench DMOS transistor cell as in Claim 16 ~~33~~ wherein the epitaxial layer has a top surface and the body region extends from the epitaxial layer's top surface into an upper portion of the epitaxial layer.

18 ~~35~~. (Amended) A trench DMOS transistor cell as in Claim 17 ~~34~~ wherein a source region is formed in said epitaxial layer.

19 ~~36~~. (Twice amended) A trench DMOS transistor cell as in Claim 18 ~~35~~ wherein the source region partially covers the body region.

#2

20 ~~37~~. (Twice amended) A trench DMOS transistor cell as in Claim 19 ~~36~~ wherein the body region includes a heavily doped portion extending upward through the epitaxial region and forming a pattern at the epitaxial layer's top surface.

21 ~~38~~. (Amended) A trench DMOS transistor cell as in Claim 20 ~~37~~ wherein the trench laterally surrounds the pattern of the heavily doped portion of the body region.

22 ~~39~~. (Amended) A trench DMOS transistor cell as in Claim 15 ~~32~~ further comprising an oxide layer on said trench side walls, said oxide layer having rounded corners along said trench.

23 ~~40~~. (Amended) A trench DMOS transistor cell as in Claim 15 ~~32~~ further comprising a gate oxide layer within the trench.

24 ~~41~~. (Twice amended) A trench DMOS transistor cell as in Claim 23 ~~40~~ further comprising electrically conducting material contiguous to the gate oxide layer, the gate oxide layer being located between the electrically conducting material and the trench.

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25 42. (Thrice amended) A trench DMOS transistor cell as in Claim 23 40 further comprising:

a first polysilicon layer on a portion of said gate oxide layer;

a second oxide layer on a portion of said first polysilicon layer;

a second polysilicon layer on a portion of said second oxide layer; and

a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

26 44. (Unchanged) A trench DMOS transistor cell as in Claim 15 32 wherein a horizontal cross section of the cell has a polygonal shape.

27 46. (Twice amended) A transistor comprising:

a first region of a first conductivity type;

a second region of a second conductivity type opposite to the first conductivity type overlying said first region;

a third region of said first conductivity type such that said first and third regions are separated by said second region;

a trench having substantially vertical side walls and extending through said third and second regions; and

a gate in said trench; wherein a portion P of said second region, which portion P is spaced from said trench, extends deeper than said trench so that, if a predetermined voltage is applied to said gate and to said third region and another predetermined voltage is applied to said first region, avalanche breakdown occurs away from a surface of said trench.

28 47. (Amended) A transistor as in Claim 27 46 wherein said portion P of said second region is more heavily doped than another portion of said second region adjacent to said trench.

29 48. (Amended) A transistor as in Claim 27 46 wherein said first region comprises a first portion and a second portion over said first portion, said second portion being more lightly doped than said first portion.

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30
~~49~~. (Unchanged) A transistor as in Claim 29 ~~48~~ wherein said avalanche breakdown is a reach-through breakdown across said second portion.

31
~~50~~. (Unchanged) A transistor as in Claim 27 ~~46~~ wherein said portion P of said second region extends deeper than said trench by more than 0.5 μm.

~~32~~
~~51~~. (Unchanged) A transistor as in Claim 27 ~~46~~ further comprising an insulator between said surface of said trench and said gate.

33
~~52~~. (Twice amended) A transistor comprising:

a first region of a first conductivity type;

a second region of said first conductivity type over said first region, said second region being more lightly doped than said first region;

a third region of a second conductivity type opposite to the first conductivity type overlying said second region, said second and third regions forming a junction;

a fourth region of said first conductivity type over said third region;

a trench having substantially vertical side walls and extending through said fourth and third regions; and

a gate in said trench; wherein a deepest part of said third region is laterally spaced from said trench; and wherein a distance between said deepest part of said third region and said first region is less than a depletion width of a planar junction which has the same doping profile as does said junction between said second and third regions at said deepest part of said third region and which is reverse biased around its breakdown voltage.

#4

34
~~53~~. (Twice amended) A transistor as in Claim 33 ~~52~~ wherein the deepest of said third region is doped more heavily than a part of said third region adjacent to said trench.

35
~~54~~. (Thrice mended) A semiconductor device comprising a semiconductor structure having a trench therein of depth d_{tr} and substantially vertical side walls, said semiconductor structure including a drain region, a source region, a body region, and a gate region within said trench and separated from said body region by dielectric material, said body region having a maximum depth d_{max} greater than said depth d_{tr}, wherein junction breakdown occurs away from said trench.

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36 55. (Amended) A semiconductor device as in Claim 35 54 further comprising a substrate of a first conductivity type and an overlying epitaxial layer of said first conductivity type, wherein said body region is of a second conductivity type opposite to said first conductivity type.

37 56. (Thrice amended) A semiconductor device as in Claim 36 55 wherein the epitaxial layer has a top surface and the body region extends from a surface of the epitaxial layer into an upper portion of the epitaxial layer.

38 57. (Amended) A semiconductor device as in Claim 36 55 wherein a source region is formed in said epitaxial layer.

39 58. (Four times amended) A semiconductor device as in Claim 36 55 wherein said body region extends upward through the epitaxial layer and forms a pattern at a surface of said epitaxial layer.

40 59. (Amended) A semiconductor device as in Claim 39 58 wherein the trench laterally surrounds the pattern of the body region.

41 60. (Amended) A semiconductor device as in Claim 35 54 further comprising an oxide layer on said trench walls, said oxide layer having rounded corners along said trench.

42 61. (Amended) A semiconductor device as in Claim 35 54 further comprising a gate oxide layer within the trench.

43 62. (Amended) A semiconductor device as in Claim 42 61 further comprising electrically conducting material contiguous to said gate oxide layer, wherein said gate oxide layer is located between said electrically conducting material and said trench.

44 63. (Twice amended) A semiconductor device as in Claim 42 61 further comprising:

a first polysilicon layer on a portion of said gate oxide layer;

a second oxide layer on a portion of said first polysilicon layer;

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a second polysilicon layer on a portion of said second oxide layer; and

a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer and providing continuity from the metal layer to the trench.

~~64.~~ 45 (Twice amended) A semiconductor device as in Claim ~~54~~ 35 further comprising three electrical contacts respectively to the gate region, the drain region, and simultaneously to the body region and the source region.

~~65.~~ 46 (Amended) A semiconductor device as in Claim ~~54~~ 35 wherein a horizontal cross section of said body region has a polygonal shape.--

#4 Concld

Enclosed is an appendix which shows how the above versions of Claims 17 - 23, 25, 26, 29 - 42, 46 - 48, and 52 - 65 are produced from the previous versions of those claims. In the appendix, added material is underlined, and deleted material is in brackets. The unchanged claims are, for the Examiner's convenience, also included in the appendix.

Add new claims 67 - 112 as follows:

--~~67.~~ 47 A trench DMOS transistor cell as in Claim ~~17~~ 1 wherein said trench laterally surrounds part of said body region.

~~68.~~ 48 A trench DMOS transistor cell as in Claim ~~17~~ 1 wherein said first and second conductivity types respectively are n-type and p-type whereby said trench DMOS transistor cell is an n-channel cell.

#5

~~69.~~ 49 A trench DMOS transistor cell as in Claim ~~30~~ 13 wherein said trench laterally surrounds part of the second covering layer.

~~70.~~ 50 A trench DMOS transistor cell as in Claim ~~30~~ 13 wherein said first and second electrical conductivity types respectively are n-type and p-type whereby said trench DMOS transistor cell is an n-channel cell.

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51 71. A trench DMOS transistor cell as in Claim 52 wherein the trench DMOS transistor cell is of the n-channel type.

52 72. A trench DMOS transistor cell as in Claim 46 wherein said trench laterally surrounds part of said second region.

53 73. A trench DMOS transistor cell as in Claim 46 wherein said first and second conductivity types respectively are n-type and p-type whereby said trench DMOS transistor cell is an n-channel cell.

54 74. A trench DMOS transistor cell as in Claim 52 wherein said trench laterally surrounds part of said third region.

55 75. A trench DMOS transistor cell as in Claim 52 wherein said first and second conductivity types respectively are n-type and p-type whereby said trench DMOS transistor cell is an n-channel cell.

#5

56 76. A trench DMOS transistor cell as in Claim 54 wherein said trench laterally surrounds part of said body region.

57 77. A trench DMOS transistor cell as in Claim 54 wherein said first and second conductivity types respectively are n-type and p-type whereby said trench DMOS transistor cell is an n-channel cell.

58 78. A vertical transistor structure comprising:

a semiconductor body comprising

(a) a drain of a first conductivity type,

(b) a body region of a second conductivity type opposite to the first conductivity type situated largely above the drain and comprising (b1) upper body material laterally surrounded by a trench that extends into the semiconductor body along its upper surface and (b2) lower body material continuous with the upper body material and extending deeper below the semiconductor body's upper surface than the trench, the drain and body region meeting each other to form a drain-body pn junction that extends to the trench, and

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(c) a source of the first conductivity type situated largely above the drain, separated from the drain by the body region, and laterally surrounded by the trench, the drain, body region, and source being of dimensions and dopants distributions suitable for causing semiconductor breakdown of the drain-body pn junction to occur away from the trench;

a gate dielectric layer comprising gate dielectric material situated in the trench along the body region; and

a gate electrode comprising gate electrode material situated in the trench and separated from the body region by the gate dielectric material.

59 ~~79~~. A structure as in Claim 58 ~~78~~ wherein the semiconductor breakdown comprises avalanche breakdown.

60 ~~80~~. A structure as in Claim 58 ~~78~~ wherein the body region extends more than 0.5 μm deeper below the semiconductor body's upper surface than the trench.

#5

61 ~~81~~. A structure as in Claim 58 ~~78~~ wherein the gate dielectric layer has a thickness of no more than 0.2 μm.

62 ~~82~~. A structure as in Claim 58 ~~78~~ wherein the gate dielectric layer consists substantially of oxide.

63 ~~83~~. A structure as in Claim 58 ~~78~~ wherein the drain comprises:

substrate drain material of a semiconductor substrate; and

epitaxial drain material of an epitaxial semiconductor layer overlying the substrate.

64 ~~84~~. A structure as in Claim 63 ~~83~~ wherein the substrate drain material is more heavily doped than the epitaxial drain material.

65 ~~85~~. A structure as in Claim 64 ~~84~~ wherein the body region and source are parts of the epitaxial layer, the trench extending into the epitaxial layer along its upper surface, the epitaxial drain material meeting the body region.

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66 ~~86.~~ A structure as in Claim 65 ~~85~~ wherein the distance from the substrate to where the body region extends deepest below the epitaxial layer's upper surface is less than the depletion width of a planar pn junction reverse biased around its reverse-bias breakdown voltage and having the same dopant concentration profile as where the epitaxial drain material meets the body region.

67 ~~87.~~ A structure as in Claim 58 ~~78~~ wherein the trench has a pair of opposing side walls that extend largely perpendicular to the semiconductor body's upper surface.

68 ~~88.~~ A structure as in Claim 58 ~~78~~ wherein the trench has an interior side wall to which the body region and source extend, the trench's interior side wall being shaped generally like a convex polygon as viewed perpendicular to the semiconductor body's upper surface.

#5

69 ~~89.~~ A structure as in Claim 68 ~~88~~ wherein the polygon is largely a regular polygon.

70 ~~90.~~ A structure as in Claim 69 ~~89~~ wherein the polygon is a hexagon.

71 ~~91.~~ A structure as in Claim 58 ~~78~~ wherein the upper body material consists of (a) a primary upper body portion directly overlying the lower body material and (b) a further upper body portion not significantly overlying any of the lower body material.

72 ~~92.~~ A structure as in Claim 71 ~~91~~ wherein the primary upper body portion is spaced laterally apart from the trench whereby, as viewed perpendicular to the semiconductor body's upper surface, the lower body material is also spaced laterally apart from the trench.

73 ~~93.~~ A structure as in Claim 68 ~~88~~ wherein the primary upper body portion is more heavily doped than the further upper body portion.

74 ~~94.~~ A structure as in Claim 58 ~~78~~ further including additional material, different from the gate electrode material, situated in the trench along the gate electrode material so as to be substantially separated from the gate dielectric material by the gate electrode material.

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75 ~~95.~~ A structure as in Claim 74 ~~94~~ wherein the additional material is dielectric material.

76 ~~96.~~ A structure as in Claim 68 ~~78~~ wherein the first and second conductivity types respectively are n-type and p-type whereby the structure is an n-channel transistor structure.

77 ~~97.~~ A vertical transistor structure comprising:

a semiconductor body comprising

(a) a drain of a first conductivity type,

(b) a body region of a second conductivity type opposite to the first conductivity type situated largely above the drain and comprising (b1) upper body material situated between a pair of trenches that extend into the semiconductor body along its upper surface and (b2) lower body material continuous with the upper body material and extending deeper below the semiconductor body's upper surface than the trenches, the drain and body region meeting each other to form a drain-body pn junction that extends to the trenches, and

(c) a source of the first conductivity type situated between the trenches largely above the drain and separated from the drain by the body region, the drain, body region, and source being of dimensions and dopant distributions suitable for causing semiconductor breakdown of the drain-body pn junction to occur away from the trenches;

a gate dielectric layer comprising gate dielectric material situated in the trenches along the body region; and

a gate electrode comprising gate electrode material situated in the trenches and separated from the body region by the gate dielectric material.

#5

78 ~~98.~~ A structure as in Claim 77 ~~97~~ wherein the semiconductor breakdown comprises avalanche breakdown.

79 ~~99.~~ A structure as in Claim 77 ~~97~~ wherein the body region extends more than 0.5 μm deeper below the semiconductor body's upper surface than the trench.

80 ~~100.~~ A structure as in Claim 77 ~~97~~ wherein the gate dielectric layer has a thickness of no more than 0.2 μm.

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81 ~~101~~. A structure as in Claim 77 ~~97~~ wherein the gate dielectric layer consists substantially of oxide.

82 ~~102~~. A structure as in Claim 77 ~~97~~ wherein the drain comprises:

substrate drain material of a semiconductor substrate; and

epitaxial drain material of an epitaxial semiconductor layer overlying the substrate.

83 ~~103~~. A structure as in Claim 82 ~~102~~ wherein the substrate drain material is more heavily doped than the epitaxial drain material.

84 ~~104~~. A structure as in Claim 83 ~~103~~ wherein the body region and source are parts of the epitaxial layer, the trenches extending into the epitaxial layer along its upper surface, the epitaxial drain material meeting the body region.

#5

85 ~~105~~. A structure as in Claim 84 ~~104~~ wherein the distance from the substrate to where the body region extends deepest below the epitaxial layer's upper surface is less than the depletion width of a planar pn junction reverse biased around its reverse-bias breakdown voltage and having the same dopant concentration profile as where the epitaxial drain material meets the body region.

86 ~~106~~. A structure as in Claim 77 ~~97~~ wherein the trenches are connected together.

87 ~~107~~. A structure as in Claim 77 ~~97~~ wherein the upper body material consists of (a) a primary upper body portion directly overlying the lower body material and (b) a further upper body portion not significantly overlying any of the lower body material.

88 ~~108~~. A structure as in Claim 87 ~~107~~ wherein the primary upper body portion is spaced laterally apart from the trenches whereby, as viewed generally perpendicular to the semiconductor body's upper surface, the lower body material is also spaced laterally apart from the trenches.

89 ~~109~~. A structure as in Claim 88 ~~108~~ wherein the primary upper body portion is more heavily doped than the further upper body portion.

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90 77
110. A structure as in Claim 97 further including additional material, different from the gate electrode material, situated in the trenches along the gate electrode material so as to be substantially separated from the gate dielectric material by the gate electrode material.

#5

91 90
111. A structure as in Claim 110 wherein the additional material is dielectric material.

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92 77
112. A structure as in Claim 97 wherein the first and second conductivity types respectively are n-type and p-type whereby the structure is an n-channel transistor structure.--

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